

92  
Concluded

10

a plurality of quadrature-phase XOR gates for multiplying the second portion of the reference-chip-sequence signal by a plurality of quadrature-phase input-data samples during the second portion of the clock cycle.--

REMARKS

By this preliminary amendment applicants amend claim 1, cancel claims 2-17, and add claims 18-25 to the application. Claims 1 and 18-25 are pending in the application.

Applicants request that this preliminary amendment be entered prior to calculating fees in the captioned application.

Respectfully submitted,

DAVID NEWMAN & ASSOCIATES, P.C.

By: Suzin C. Bailey

Date: January 9, 1998

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